Integrated Circuit Test Tools

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Calendar

	Morning session		Afternoon session	
Date	**Responsible (Schedule)**	**Unit**	**Responsible/ (Schedule)**	**Unit**
Monday 8/09	L. Parrilla E. Castillo (10:00-13:00)	Introduction to integrated circuit testing		
Tuesday 9/09	L. Parrilla A. García (10:00-13:30)	Deterministic testing of digital circuits I		
Wednesday 10/09	L. Parrilla A. García (10:00-14:00)	Deterministic testing of digital circuits II		
Thursday 11/09	L. Parrilla A. García (10:00-13:30)	Deterministic testing of digital circuits III		

Calendar

	Morning session		Afternoon session	
Date	**Responsible (Schedule)**	**Unit**	**Responsible/ (Schedule)**	**Unit**
Friday 12/09	A. García E. Castillo (10:00-13:30)	Design for test I		
Monday 15/09	A. García E. Castillo (10:00-14:00)	Design for test II		
Tuesday 16/09	L. Parrilla A. García E. Castillo (10:00-14:00)	Fault-tolerant design I		

Calendar

	Morning session		Afternoon session	
Date	**Responsible (Schedule)**	**Unit**	**Responsible/ (Schedule)**	**Unit**
Wednesday 17/09	A. García E. Castillo (10:00-14:00)	Fault-tolerant design II		
Thursday 18/09	L. Parrilla A. García E. Castillo (10:00-14:00)	CAD tools for test and design for test I		
Friday 19/09	L. Parrilla A. García E. Castillo (10:00-14:00)	CAD tools for test and design for test II		

Content

- Introduction to Integrated Circuit Testing:
  - Importance of testing.
  - Reliability: Failure rate and mean time between failures.
  - Partitioning.
  - Defect models.

- Deterministic Testing of Digital Circuits:
  - Testing of Combinational Circuits: Path Sensitization (Theoretical Overview and Simulation Exercises).
  - Testing of Sequential Circuits: State Table-Based Testing and Gate-Level Testing (Theoretical Overview and Simulation Exercises).
  - Testing of RAM.
  - Random testing.
  - Simulation exercises.

Content

- Design for test:
  - Combinational design.
  - Design for scan test and self-test.
  - Built-In self-test.
  - Mixed-Signal circuits.
  - Debug and Verification Cores in Programmable Devices.
  - Simulation and practical exercises.

- Fault-tolerant design:
  - Static redundancy.
  - Dynamic redundancy.
  - Hybrid redundancy.
  - Fault tolerant in RAM.
  - Simulation exercises.

Content

- CAD tools for test and design for test:
  - Use of CAD Tools for Testing of Digital and Mixed-Signal Integrated Circuits.
  - CAD Tools for Design for Test.
  - Practical exercises.